

FIG. 1 is a block diagram of a video signal processing system. The system includes a video signal input, a timing controller, a signal processor, a horizontal signal processor, and a display panel. The video signal input provides Hsync, Vsync, and video signal data to a signal absence detector (60). The signal absence detector outputs a signal to a timing controller (70). The timing controller (70) includes a one-shot multi-vibrator (71) and a signal processor (75). The one-shot multi-vibrator (71) is connected to a timing capacitor (MG) and a timing resistor (POWC). The signal processor (75) outputs Vs and Gs signals to the horizontal signal processor (16). The horizontal signal processor (16) outputs Vs, Gs, and data signals to the display panel (100). The display panel (100) includes a gate driver (12) and a data driver (10). The gate driver (12) includes a gate driver circuit (G1, G2) and a gate driver control circuit (DPR, CK, CLR). The data driver (10) includes a data driver circuit (DPR, CK, CLR) and a data driver control circuit (DPR, CK, CLR).

FIG. 1

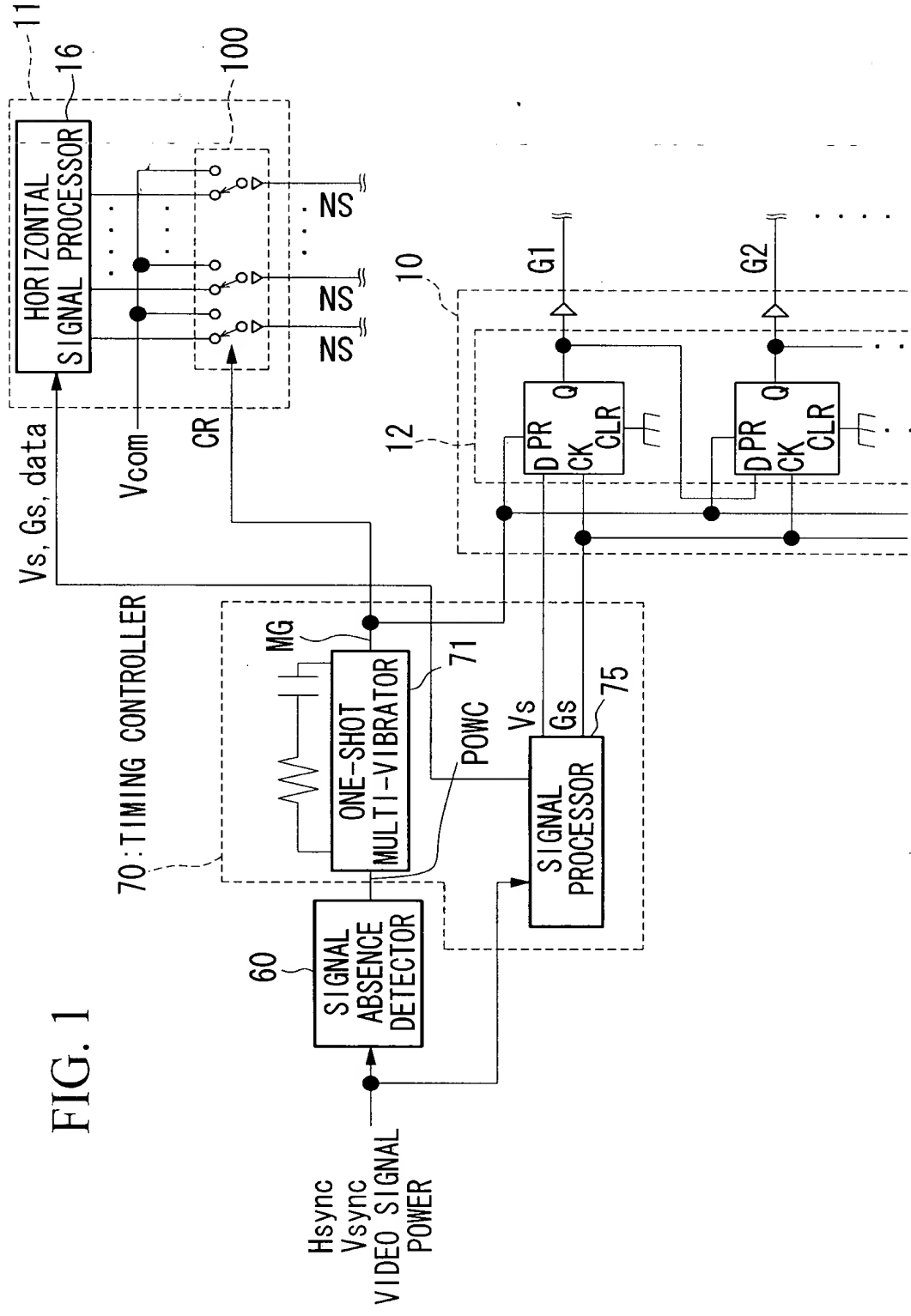


FIG. 2

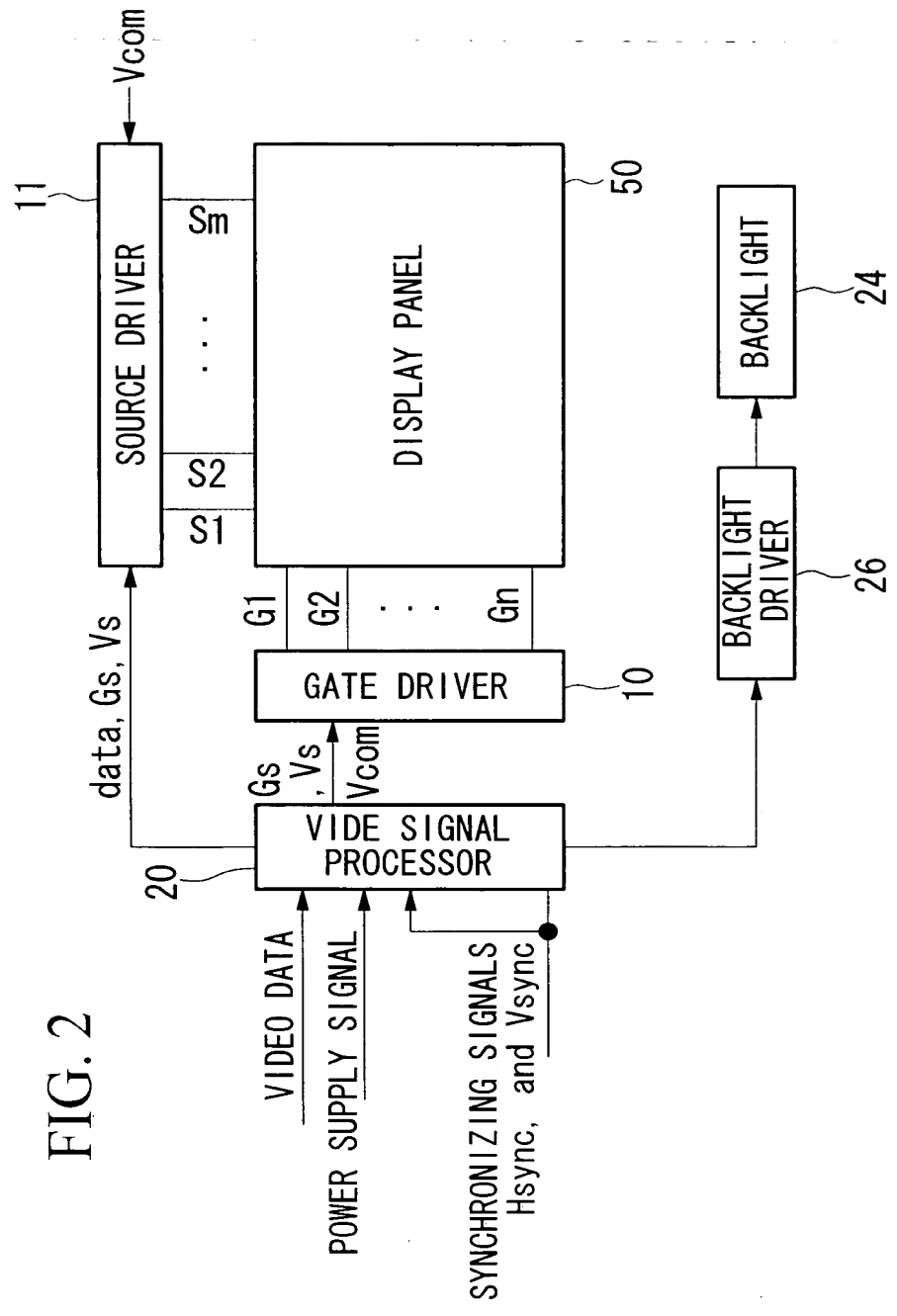


FIG. 3A

Hsync

FIG. 3B

Vsync

FIG. 3C

POWC

FIG. 3D

MG

FIG. 3E

G1
G2
⋮
Gn

FIG. 3F

S_i
($i=1 \sim m$)

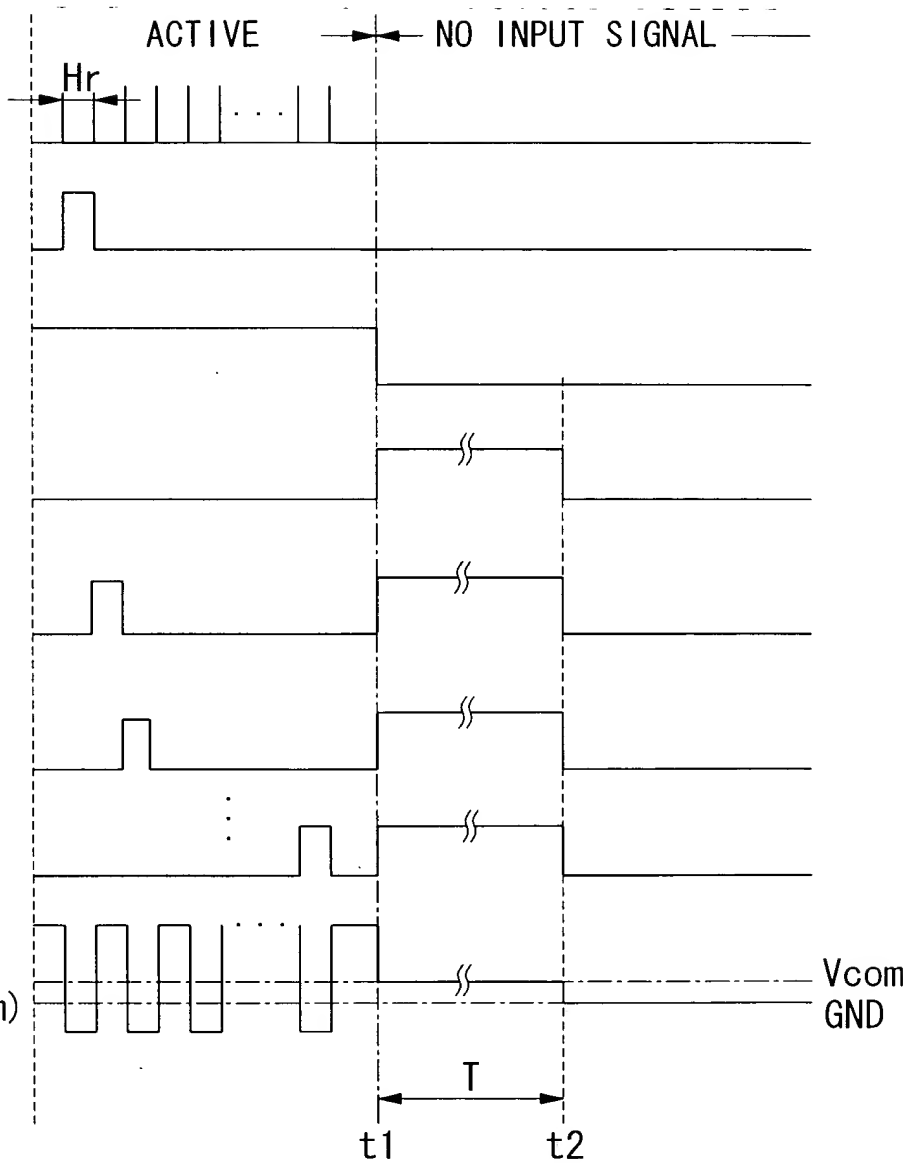


FIG. 4

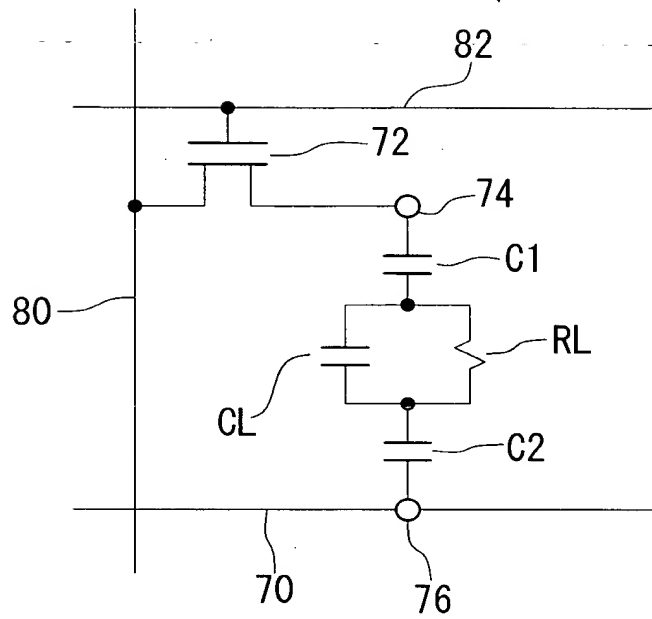


FIG. 5

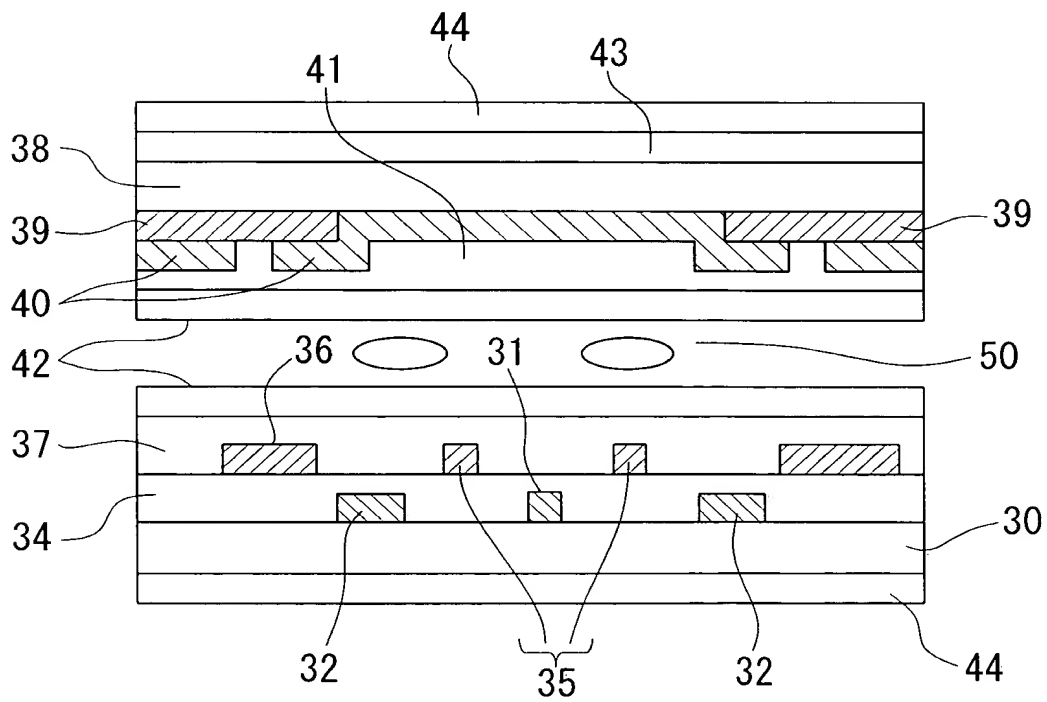


FIG. 6

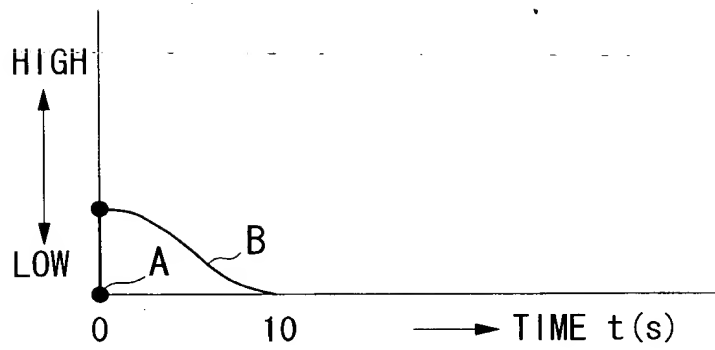


FIG. 7A

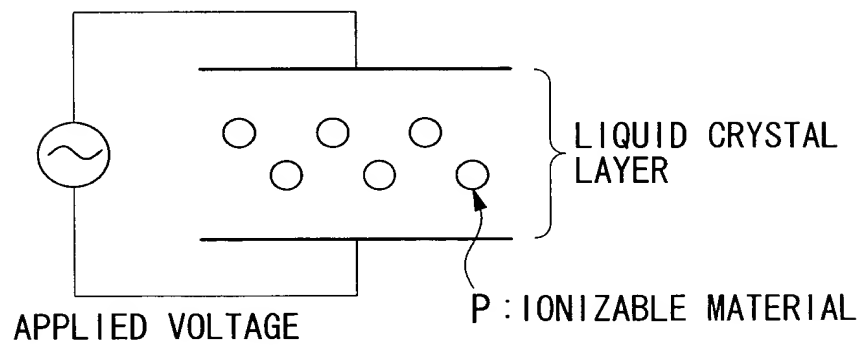


FIG. 7B

